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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,441	06/02/2000	Slobodan Nedic	P/3341-8	7204

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EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,441	NEDIC, SLOBODAN	
	Examiner	Art Unit	
	Kevin M Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the amendment filed 12/22/2003, is a non-final office action.

Response to Arguments

2. The previous objection to the specification is withdrawn.

3. Applicant's arguments filed 12/22/2003 regarding claims 1-20 and 28-43 have been fully considered but they are not persuasive.

The rejections of claims 1-20 and 28-43 are maintained because claims 1-20 and 28-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Nedic et al (US 6,563,841). The applied reference has a common assignment and one common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Applicant's arguments, see amendment received 12/22/2003, with respect to the rejections of claims 21-27 and 44-50 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Harikumar et al (US 6,631,175) in view of Ono et al (US 6,302,576).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-20 and 28-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Nedic et al (US 6,563,841).

Regarding claim 1, Nedic discloses a discrete multi-tone receiver circuit for providing a decoded output (column 6, lines 53-64 and figure 3). The transmission channel will have noise (interference) present (column 8, lines 17-33). The receiver operates on a digital subscriber line (column 1, lines 17-23). The receiver comprises a first stage, which has a frequency response for applying a discrete Fourier transform to the input (column 7, lines 25-30 and figure 3, element 106). The receiver has a second stage, which receives the output of the first stage (figure 3) and per-bin decodes (column 3, line 66 to column 4, line 10) the signal based on a MLSE algorithm (column 5, lines 51-53 and figure 3, element 112) to recover the data (output bits in figure 3). A time domain windowing stage applies time domain windowing to the input signal prior to the first stage (column 7, lines 25-30 and figure 3, element 104).

Regarding claim 2, Nedic discloses a time domain equalizing stage prior to the time domain windowing stage as shown in figure 1 and column 6, lines 53-64.

Regarding claim 3, Nedic discloses the signal at node r(n), which is prior to the time domain windowing stage, is output from the time domain equalizing stage (column 6, lines 53-64).

Regarding claim 4, Nedic discloses the windowing stage employs the Hanning type window (column 4, lines 24-25).

Regarding claim 5, Nedic discloses a per-bin equalizing stage (column 1, lines 17-22 and figure 3, element 110).

Regarding claim 6, Nedic discloses the per-bin equalizing stage comprises a bank of equalizers (figure 3, element 110) and the bank of equalizers corresponds to the active bins of the output from the first stage (column 1, lines 17-22 and figure 3).

Regarding claim 7, Nedic discloses the equalizer 110 comprises a feed forward filter 114 shown on figure 4 and filter 114 is a FIR filter (column 9, lines 20-39).

Regarding claim 8, Nedic discloses the PRS decoder of figure 3, applies PRS decoding bin-by-bin along the frequency axis in the digital data (column 9, line 60 to column 10, line 7).

Regarding claim 9, Nedic discloses the PRS decoder includes a MLSE (column 5, lines 51-53). The MLSE operates an "exhaustive" operation each time it operates.

Regarding claim 10, Nedic discloses the PRS decoder includes a Viterbi decoder (column 5, lines 51-53).

Regarding claim 11, Nedic discloses a discrete multi-tone receiver circuit for providing a decoded output (column 6, lines 53-64 and figure 3). The transmission channel will have noise (interference) present (column 8, lines 17-33). The receiver operates on a digital subscriber line (column 1, lines 17-23). The receiver comprises a first stage, which has a frequency response for applying a discrete Fourier transform to the input (column 7, lines 25-30 and figure 3, element 106). The receiver has a second stage, which receives the output of the first stage (figure 3) and per-bin decodes (column 3, line 66 to column 4, line 10) the signal based on a MLSE algorithm (column 5, lines 51-53 and figure 3, element 112) to recover the data (output bits in figure 3). A frequency domain windowing stage is disposed between the first and second stages (column 5, line 54 to column 6, line 9).

Regarding claim 12, Nedic discloses a time domain windowing stage applies time domain windowing to the input signal prior to the first stage (column 7, lines 25-30 and figure 3, element 104).

Regarding claim 13, Nedic discloses a per-bin equalizing stage (column 1, lines 17-22 and figure 3, element 110).

Regarding claim 14, Nedic discloses the per-bin equalizing stage comprises a bank of equalizers (figure 3, element 110) and the bank of equalizers corresponds to the active bins of the output from the first stage (column 1, lines 17-22 and figure 3).

Regarding claim 15, Nedic discloses the equalizer 110 comprises a feed forward filter 114 shown on figure 4 and filter 114 is a FIR filter (column 9, lines 20-39).

Regarding claim 16, Nedic discloses the output to the FFT is input to a frequency domain windowing circuit and then to an equalizer circuit (column 5, line 54 to column 6, line 9).

Regarding claim 17, Nedic discloses the PRS decoder of figure 3, applies PRS decoding bin-by-bin along the frequency axis in the digital data (column 9, line 60 to column 10, line 7).

Regarding claim 18, Nedic discloses the PRS decoder includes a MLSE (column 5, lines 51-53). The MLSE operates an "exhaustive" operation each time it operates.

Regarding claim 19, Nedic discloses the PRS decoder includes a Viterbi decoder (column 5, lines 51-53).

Regarding claim 20, Nedic discloses the windowing stage employs the Hanning type window (column 4, lines 24-25).

Regarding claim 28, Nedic discloses a method of using a discrete multi-tone receiver circuit for providing a decoded output (column 6, lines 53-64 and figure 3). The transmission channel will have noise (interference) present (column 8, lines 17-33). The receiver operates on a digital subscriber line (column 1, lines 17-23). A time domain windowing stage applies time domain windowing to the input signal prior to the first stage (column 7, lines 25-30 and figure 3, element 104). The receiver applies a discrete Fourier transform to the input (column 7, lines 25-30 and figure 3, element 106). The receiver receives the output of the Fourier transform (figure 3) and per-bin decodes (column 3, line 66 to column 4, line 10) the signal based on a MLSE algorithm (column 5, lines 51-53 and figure 3, element 112) to recover the data (output bits in figure 3).

Regarding claim 29, Nedic discloses a time domain equalizing step prior to the Fourier transform step as shown in figure 1 and column 6, lines 53-64.

Regarding claim 30, Nedic discloses a time domain equalizing step prior to the time domain windowing stage as shown in figure 1 and column 6, lines 53-64.

Regarding claim 31, Nedic discloses the windowing step employs the Hanning type window (column 4, lines 24-25).

Regarding claim 32, Nedic discloses the output to the FFT is input an equalizer circuit (column 5, line 54 to column 6, line 9) and the output of the equalizer is input to the PRS decoder stage (figure 3).

Regarding claim 33, Nedic discloses the PRS decoder of figure 3, applies PRS decoding bin-by-bin along the frequency axis in the digital data (column 9, line 60 to column 10, line 7).

Regarding claim 34, Nedic discloses the PRS decoder includes a MLSE (column 5, lines 51-53). The MLSE operates an "exhaustive" operation each time it operates.

Regarding claim 35, Nedic discloses the PRS decoder includes a Viterbi decoder (column 5, lines 51-53).

Regarding claim 36, Nedic discloses a method of using a discrete multi-tone receiver circuit for providing a decoded output (column 6, lines 53-64 and figure 3). The transmission channel will have noise (interference) present (column 8, lines 17-33). The receiver operates on a digital subscriber line (column 1, lines 17-23). The receiver applies a discrete Fourier transform to the input (column 7, lines 25-30 and figure 3, element 106). Frequency domain windowing is applied to the output of the discrete

Fourier transform (column 5, line 54 to column 6, line 9). The receiver receives the output of the frequency domain windowing circuit (column 5, line 54 to column 6, line 9) and per-bin decodes (column 3, line 66 to column 4, line 10) the signal based on a MLSE algorithm (column 5, lines 51-53 and figure 3, element 112) to recover the data (output bits in figure 3).

Regarding claim 37, Nedic discloses a time domain equalizing step prior to the Fourier transform step as shown in figure 1 and column 6, lines 53-64.

Regarding claim 38, Nedic discloses the output to the FFT is input an equalizer circuit (column 5, line 54 to column 6, line 9) and the output of the equalizer is input to the PRS decoder stage (figure 3).

Regarding claim 39, Nedic discloses the output to the FFT is input to a frequency domain windowing circuit and then to an equalizer circuit (column 5, line 54 to column 6, line 9).

Regarding claim 40, Nedic discloses the PRS decoder of figure 3, applies PRS decoding bin-by-bin along the frequency axis in the digital data (column 9, line 60 to column 10, line 7).

Regarding claim 41, Nedic discloses the PRS decoder includes a MLSE (column 5, lines 51-53). The MLSE operates an "exhaustive" operation each time it operates.

Regarding claim 42, Nedic discloses the PRS decoder includes a Viterbi decoder (column 5, lines 51-53).

Regarding claim 43, Nedic discloses the windowing step employs the Hanning type window (column 4, lines 24-25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-27 and 44-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harikumar et al (US 6,631,175) in view of Ono et al (US 6,302,576).

Regarding claims 21 and 44, Harikumar discloses a receiver circuit that provides a decoded output from a received discrete multi-tone modulated input signal (title and figure 1). The input signal is received from a communication channel having noise thereon (column 1, line 58 to column 2, line 6). The DMT system receives digital data (figure 1, element 80). The method applies a discrete Fourier transform to the input signal. This is shown in figure 1 since the output of the channel is the input to the DFT. The input data is decoded (element 140) after the noise at each frequency bin has been removed (column 6, line 53 to column 7, line 17). Harikumar does not disclose using a maximum likelihood sequence estimation (MSLE) algorithm to recover the received data. Ono discloses using a MLSE where the MLSE unit calculates metrics corresponding to a transmitted symbol sequence estimated by an adaptive equalizer (abstract). The adaptive equalizer is a MLSE equalizer (column 1, lines 41-45). The MLSE equalizer passes a received and digitized signal through a matched filter which minimizes the influence of noise by changing the characteristics thereof in accordance with the transmission path characteristics so that the most likely transmitted symbol

sequence is estimated from the output of the matched filter (column 1, lines 45-54). Therefore, the noise components are subtracted and cancelled from the received signal by adjusting the coefficients (column 7, lines 29-50). It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the teachings of Ono in the decoder of Harikumar. In high speed digital communications, the transmission path characteristics thereof largely fluctuates with time due to frequency selective fading caused by multi-path transmissions and to correctly restore the originally transmitted symbols from the received signal, the adaptive equalizer, comprising the MLSE, of Ono is used (column 1, lines 36-40).

Regarding claims 22 and 45, when the transmission path characteristics for each bin or channel are the same, the coefficients will be equal.

Regarding claims 23 and 46, when the transmission path characteristics for each bin or channel are different, the coefficients will be different.

Regarding claims 24 and 47, Ono discloses utilizing the MLSE algorithm to perform cancellation of noise as described above.

Regarding claim 25, Harikumar discloses the noise components are added to the system when through noise bleeding (column1, lines 57-65) and noise is white noise or other noise signals (column 6, lines 40-52).

Regarding claims 26 and 49, the windowing procedure can be time domain windowing (column 6, lines 19-25).

Regarding claims 27 and 50, the windowing procedure can be frequency domain windowing (figure 1, element 130).

Contact Information

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry or for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Burd, whose telephone number is (703) 308-7034. The Examiner can normally be reached on Monday-Thursday from 9:00 AM - 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Kevin M. Burd
PATENT EXAMINER
2/24/2004